CLAIMS

What is Claimed is:

1. An embedded disk controller having a servo controller, comprising:

a servo controller interface with a speed matching module and a pipeline control module such that at least two processors share memory mapped registers without conflicts.

2. The controller of Claim 1, where one processor operates at a first frequency and a second processor operates at the second frequency.

3. The controller of Claim 1, where the servo-controller and the servo controller interface operate in same or different frequency domains.

4. The controller of Claim 1, the speed matching module ensures communication without inserting wait states in a servo controller interface clock domain for write access to the servo controller.

5. The controller of Claim 1, where there is no read conflicts between the first and second processor.

6. The controller of Claim 1, provides a hardware mechanism for indivisible register access to the first or second processor.

7. The controller of Claim 6, where the hardware mechanism includes a hard semaphore.

9. The controller of Claim 6, where the hardware mechanism includes a soft semaphore.

10. The controller of Claim 1, where the pipeline control module resolves conflict between the first and second processor transaction.

11. The controller of Claim 1, where the first and second processor communicate with the servo controller via two separate buses.

12. The controller of Claim 1, where if there is a write conflict between the first and second processor, pipeline control module holds write access to the second processor.

13. The controller of Claim 6, where the hardware mechanism is a semaphore register.

14. A system for reading and writing data to a storage medium, comprising:

an embedded disk controller having a servo controller interface module that includes a speed matching module and a pipeline control module such that at least two processors share memory mapped registers without conflicts.

15. The system of Claim 14, where one processor operates at a first frequency and a second processor operates at the second frequency.

16. The system of Claim 14, where the servo-controller and the servo controller interface operate in same or different frequency domains.

17. The system of Claim 14, the speed matching module ensures communication without inserting wait states in a servo controller interface clock domain for write access to the servo controller.

18. The system of Claim 14, where there is no read conflicts between the first and second processor.

19. The system of Claim 14, provides a hardware mechanism for indivisible register access to the first or second processor.

20. The system of Claim 19, where the hardware mechanism includes a hard semaphore.

21. The system of Claim 19, where the hardware mechanism includes a soft semaphore.

22. The system of Claim 14, where the pipeline control module resolves conflict between the first and second processor transaction.

23. The system of Claim 14, where the first and second processor communicate with the servo controller via two separate buses.

24. The controller system of Claim 14, where if there is a write conflict between the first and second

processor, pipeline control module holds write access to the second processor.

25. The system of Claim 19, where the hardware mechanism is a semaphore register.